Nikolaos K. Kavvadias, Ph.D., M.Sc., B.Sc.

Personal information

Date of birth	April 29, 1977
Residence	Kornarou 12 Rd., Nea Ampliani, 35100 Lamia, Greece
Phone (land.)	+30-22310-43765
Phone (mob.)	+30-6972-673106
E-mail	nikos@nkavvadias.com nikolaos.kavvadias@gmail.com
Website	http://www.nkavvadias.com/
LinkedIn	http://gr.linkedin.com/pub/nikolaos-kavvadias/16/811/358
Github	http://github.com/nkkav/
Skype ID	nikolaos.kavvadias
Twitter ID	nkkav
Military service	Fulfilled
Driving license	Class B

Current occupation

Independent consultant – Research scientist

Work experience

01/2014-today	Independent consultant providing hardware/software development, design, consulting and support services (EDA tools, system/processor IP, ASIC/FPGA).
06/2014-09/2014	Programming and consulting services for an undisclosed US-based company offering compiler technology for GPGPU/high-performance computing.
09/2011-12/2013	FP7-STREP **ALMA**: "Architecture oriented paraLlelization for high performance embedded Multicore systems using scilAb" EU research program. • Developed **aprof**, a performance estimator and **hlo,** a high-level optimizer.
01/2010-12/2012	FP7-IST **ENOSYS**: "intEgrated modelliNg and synthesis tOol flow for embedded SYStems design" EU research program. • Developed **txlcopt**, a source-to-source transformation tool for arithmetic and loop optimizations for ANSI C, written in TXL.
09/2008-06/2012	Visiting lecturer at the Dept. of Informatics and Telecommunications of the University of Peloponnese, Greece. • Taught the following courses: VHDL, Verilog HDL, Compilers I/II, Computer Architecture II, Digital Circuit Design. Supervision of students' theses.
06/2007, 02/2008	FPGA laboratory, Electronic Physics M. Sc. Program, Dept. of Physics, Aristotle University of Thessaloniki (AUTH). Developed a number of FPGA assignments.
01/2005-12/2007	Successful grant proposal co-author/researcher (131,500 EUR): "Development of a methodology for the design of optimal application-specific processors" funded by the Greek Secretariat of Research and Technology (GSRT).
09/2001-08/2003	Laboratory assistant at the Electronics Lab of the Dept. of Physics at AUTH.
09/2001-02/2003	FP5-IST **EASY**: "Energy-Aware System-on-Chip design of the HIPERLAN/2 standard" funded by the EU. • Energy consumption modeling of ARM processor chips.

08/2000-07/2001	Research assistant for the project: "Memory management methodology for real-time and low-power embedded multimedia systems" funded by the GSRT. • Signal processing and bus encoding schemes for SoC energy reduction.

Studies

03/2003-05/2008	Ph.D. degree ("**Excellent**") from the Physics Dept. of AUTH on the "Development of an application-specific processor design methodology".
1999-2002	M.Sc. on Electronic Physics from AUTH, Greece. Grade: **9.41**/10.
1995-1999	B.Sc. on Physics from AUTH, Greece. Grade: **8.22**/10.

Background knowledge

Prog. languages	C, C++, Pascal, Tcl/Tk, TXL, HTML, XML, MATLAB, Processing.
HDLs/ADLs	Verilog HDL, VHDL, SystemC, LISA 2.0, nML, ArchC.
Assembly	ARMv4 (ARM7TDMI), MIPS-I/MIPS32, PicoBlaze, ASIPs.
Software devel. tools	GCC, LLVM, Machine-SUIF, lex/flex, yacc/bison, awk, bash, binutils, newlib, GDB, Graphviz, gnuplot, gmplib, TXL environment, Boost libraries, SALTO, git/svn, Valgrind, delta/creduce; open-source tools and libraries.
EDA tools	Xilinx ISE/ISim and Vivado/Vivado HLS, Mentor Modelsim, GHDL, GTKwave, Icarus Verilog, Synopsys VCS/DVE, Aldec Active-HDL, VHDLSimili, Synplify ASIC, Mentor LeonardoSpectrum, Prover eCheck, PSPICE.
Development boards	Xilinx Spartan-3/3E/3AN Starter Kit FPGA boards, ARM Evaluator, ARM Integrator, Altera Nios-II Development Kit, Adapteva Parallela.
OS	Linux (Fedora, Redhat, Ubuntu), Cygwin/MinGW, MS Windows (95/98/XP/7).
Desktop suites	MS Office/Visio, LibreOffice, Virtual PC, VMware, LaTeX2e, TeXmaker.

Languages

English	FCE level. Extensive experience in academic and technical writing.

Appointments, awards and distinctions

2002-today	110 citations to his research work. (h-index = 6)
2001-today	9 journal and 26 conference publications, 1 book chapter and significant contribution to 8 technical reports (deliverables) for EU FP5/FP7 projects.
2005-today	Reviewer for international research journals and conferences including ACM and IEEE Transactions, IET periodicals, DATE (2005-2008), FPL (2010-2013).
2004	Scholarship of excellence (3,200 EUR) of the Research Committee of the Aristotle University of Thessaloniki for the year 2004.
1999-2000	1st place and corresponding financial award (equivalent to 1,760 EUR) after the completion of the 1st year of his postgraduate studies.
10/1999	1st place in the selection process to the Electronic Physics M.Sc. program at the Dept. of Physics, AUTH, Greece.

Selection of development projects, prototypes and products

- The **HercuLeS** high-level synthesis tool: http://www.nkavvadias.com/hercules/
- The **YARDstick** custom instruction generator for ASIPs: http://www.nkavvadias.com/yardstick/
- The **ByoRISC** extensible soft core processor supporting multi-input, multi-output custom instructions: http://www.nkavvadias.com/misc/byorisc-demo-0.0.1.zip
- **loopgen:** VHDL IP cores for implementing nested loop structures: http://nkavvadias.com/eshop/index.php?id_product=10&controller=product
- **xmodz:** Fast hardware implementations of integer modulo: http://nkavvadias.com/eshop/index.php?id_product=9&controller=product
- **kdiv** and **kmul:** C/assembly code generators for integer division and multiplication by constant: http://sourceforge.net/projects/kdiv/ and http://sourceforge.net/projects/kmul/
- **llvmparse:** Portable, standalone, parsers for the textual LLVM IR: http://nkavvadias.com/eshop/index.php?id_product=8&controller=product
- **kvcordic:** Universal multi-mode CORDIC computer: http://www.opencores.org/project,kvcordic
- **aprof:** IR profiler tool. http://www.nkavvadias.com/doc/aprof/aprof-README.html
- **hlo:** C-to-C source code optimizer. http://www.nkavvadias.com/doc/hlo/hlo-README.html
- FPGA designs for teaching or demonstration including: line/circle drawing IPs, LCD messaging machine with Picoblaze, two-player game with LED display and UART I/O interface, 2D cellular automata evolution, generic image/video synthesis engine, image viewer, imaging processor.
- FPGA designs for customers incl. MSF60/DCF77 receiver, biomedical signal processor, FFT IP.

Ten most important peer-reviewed publications (out of a total of 36)

1. **N. Kavvadias**, P. Neofotistos, S. Nikolaidis, K. Kosmatopoulos and T. Laopoulos, "Measurements Analysis of the Software-Related Power Consumption in Microprocessors," IEEE Transactions on Instrumentation and Measurement, Vol. 53, No. 4, pp. 1106-1112, Aug. 2004.
2. **N. Kavvadias** and S. Nikolaidis, "Zero-overhead loop controller for implementing multimedia algorithms," IEE Proc. – Computers & Digital Techniques, Vol. 152, No. 4, pp. 517-526, Jul. 2005.
3. **N. Kavvadias**, V. Giannakopoulou, and S. Nikolaidis, "Development of a customized processor architecture for accelerating genetic algorithms," Microprocessors and Microsystems, Vol. 31, Issue 5, pp. 347-359, Aug. 2007.
4. **N. Kavvadias**, S. Nikolaidis, "Elimination of overhead operations in complex loop structures for embedded microprocessors," IEEE Trans. on Computers, Vol. 57, No. 2, pp. 200-214, Feb. 2008.
5. **N. Kavvadias** and S. Nikolaidis, "Automated Instruction-Set Extension of Embedded Processors with Application to MPEG-4 Video Encoding," Proc. 16th IEEE Int. Conf. on Application-specific Systems, Architectures and Processors (ASAP), pp. 140-145, Samos, Greece, July 23-25, 2005.
6. **N. Kavvadias** and S. Nikolaidis, "A flexible instruction generation framework for extending embedded processors," in Proceedings of the 13th IEEE Mediterranean Electrotechnical Conference (MELECON 2006), pp. 125-128, Benalmadena (Malaga), Spain, May 16-19, 2006.
7. **N. Kavvadias** and S. Nikolaidis, "The ByoRISC configurable processor family," Proceedings of the IFIP/IEEE VLSI-SoC 2008, pp. 439-444, Rhodes Island, Greece, October 13-15, 2008.
8. **N. Kavvadias** and K. Masselos, "Automated synthesis of FSMD-based accelerators for hardware compilation," Proc. 2012 IEEE 23rd Int. Conf. on Application-Specific Systems, Architectures and Processors (ASAP), pp. 157-160, Delft, The Netherlands, July 9-11, 2012.
9. **N. Kavvadias** and K. Masselos, "Hardware design space exploration using HercuLeS HLS," Proc. 17th Panhellenic Conf. on Informatics with International Participation (PCI 2013), pp. 195-202, Sep. 19-21, 2013, Thessaloniki, Greece.
10. **N. Kavvadias**, V. Giannakopoulou and K. Masselos, "FSMD-Based Hardware Accelerators for FPGAs," in Embedded Systems - Theory and Design Methodology, ISBN 978-953-51-0167-3, ed. by Kiyofumi Tanaka, Intech, pp. 143-166, Mar. 2012.