Nikolaos K. Kavvadias, Ph.D., M.Sc., B.Sc.

Personal information

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Military service	Fulfilled
Driving license	Class B

Current occupation

Independent consultant – Research scientist

Work experience

01/2014-today	Independent consultant providing hardware/software development, design, consulting and support services (EDA tools, system/processor IP, ASIC/FPGA).
01/2012-today	Cofounder of Ajax Compilers (http://www.ajaxcompilers.com), a high-tech startup marketing the HercuLeS high-level synthesis environment and offering hardware and software compilation services..
06/2014-09/2014	Programming and consulting services for an undisclosed US-based company offering compiler technology for GPGPU/high-performance computing.
09/2011-12/2013	FP7-STREP **ALMA**: "Architecture oriented paraLlelization for high performance embedded Multicore systems using scilAb" EU research program. • Developed **aprof**, a performance estimator working at the compiler intermediate representation (IR) level. **aprof** allows to quickly identify application hotspots. It works by executing the instrumented application IR as a compiled application simulator. • Developed **hlo,** a source-to-source optimizer for ANSI C. **hlo** supports generic restructuring transformations, and loop-specific and arithmetic optimizations that can be applied as self-contained passes directly to C code.
01/2010-12/2012	FP7-IST **ENOSYS**: "intEgrated modelliNg and synthesis tOol flow for embedded SYStems design" EU research program. • Developed **txlcopt**, a source-to-source transformation tool for arithmetic and loop optimizations for ANSI C, written in TXL.
09/2008-06/2012	Visiting lecturer at the Dept. of Informatics and Telecommunications of the University of Peloponnese, Greece. • Taught the following courses: VHDL, Verilog HDL, Compilers I/II, Computer Architecture II, Digital Circuit Design. • Supervision of students' B.Sc. and M.Sc. theses.

06/2007, 02/2008	FPGA laboratory, Electronic Physics M. Sc. Program, Dept. of Physics, Aristotle University of Thessaloniki (AUTH). Developed a number of FPGA assignments.
01/2005-12/2007	Successful grant proposal co-author and researcher (131,500 EUR): "Development of a methodology for the design of optimal application-specific processors" funded by the Greek Secretariat of Research and Technology (GSRT).
09/2001-08/2003	Laboratory assistant at the Electronics Lab of the Dept. of Physics at AUTH.
09/2001-02/2003	FP5-IST **EASY**: "Energy-Aware System-on-Chip design of the HIPERLAN/2 standard" funded by the EU. • Energy consumption modeling of ARM processor chips based on measuring the instantaneous current drawn by the processor. Co-developed an accurate model that accounted for the inter-instruction effect on energy (variations in energy consumption due to consecutive instructions' pairing). The model has been validated within 3-6% accuracy by independent researchers and industrial R&D groups in the US, Europe and Asia.
08/2000-07/2001	Research assistant for the project: "Memory management methodology for real-time and low-power embedded multimedia systems" funded by the GSRT. • Explored on-chip bus encoding schemes such as Gray and T0 encoding for SoC energy reduction focusing on data bus transfers to and from memory.

Studies

03/2003-05/2008	Ph.D. degree ("**Excellent**") from the Physics Dept. of AUTH on the "Development of an application-specific processor design methodology". • Developed a comprehensive methodology for the design of the instruction repertoire and the microarchitecture of application-specific instruction-set processors (ASIPs). • Novel zero-overhead looping technique for arbitrary loop nests decided at instruction fetch. • Developed the ByoRISC ASIP. ByoRISC compares favorably in terms of application execution time to soft-core processors like Nios-II and even to VLIWs similar to HP's VEX. • Developed the YARDstick retargetable custom instruction generation tool.
10/1999-10/2002	M.Sc. on Electronic Physics from AUTH, Greece. Grade: **9.41**/10. • M.Sc. thesis subject: "Development and digital design of parametric architectures for multimedia processing".
09/1995-10/1999	B.Sc. on Physics from AUTH, Greece. Grade: **8.22/**10. • B.Sc. thesis subject: "Study of the transition activity in alternative digital multiplier architectures – Digital design".

Background knowledge

Programming languages	C, C++, Pascal, Tcl/Tk, TXL, HTML, XML, MATLAB, Processing.
HDLs/ADLs	Verilog HDL, VHDL, SystemC, LISA 2.0, nML, ArchC.
Assembly	ARMv4 (ARM7TDMI), MIPS-I/MIPS32, PicoBlaze, ASIPs.

Software devel. tools	GCC, LLVM, Machine-SUIF, lex/flex, yacc/bison, awk, bash, binutils, newlib, GDB, Graphviz, gnuplot, gmplib, TXL environment, Boost libraries, SALTO, git/svn, Valgrind, delta/creduce; open-source tools and libraries.
EDA tools	Xilinx ISE/ISim, Xilinx Vivado/Vivado HLS, Mentor Modelsim, GHDL, GTKwave, Icarus Verilog, YOSYS, Synopsys VCS/DVE, Aldec Active-HDL, VHDLSimili, Synplify ASIC, Mentor LeonardoSpectrum, Prover eCheck, PSPICE.
Development boards	Xilinx Spartan-3/3E/3AN Starter Kit FPGA boards, ARM Evaluator, ARM Integrator, Altera Nios-II Development Kit, Adapteva Parallela.
OS	Linux (Fedora, Redhat, Ubuntu), Cygwin/MinGW, MS Windows (95/98/XP/7).
Desktop suites	MS Office/Visio, LibreOffice, Virtual PC, VMware, LaTeX2e, TeXmaker.

Languages

English	FCE level. Extensive experience in academic and technical writing.

Appointments, awards and distinctions

2002-today	110 citations to his research work. (h-index = 6)
2001-today	10 journal, 26 conference publications, 1 book chapter, 2 informal publications and significant contribution to 8 technical reports (deliverables) for EU FP5/FP7 projects.
2005-today	Reviewer for international research journals and conferences including ACM and IEEE Transactions, IET periodicals, DATE (2005-2008), FPL (2010-2013).
09/2013	Co-chair of the FPL 2013 High-level synthesis BoF (Birds of a Feather) session.
2004	Scholarship of excellence (3,200 EUR) of the Research Committee of the Aristotle University of Thessaloniki for the year 2004.
1999-2000	1st place and corresponding financial award (equivalent to 1,760 EUR) after the completion of the 1st year of his postgraduate studies.
10/1999	1st place in the selection process to the Electronic Physics M.Sc. program at the Dept. of Physics, AUTH, Greece.

R&D interests

- Development of a methodology for automating the design of the instruction set architecture and microarchitecture of application-specific processors that is based on application analysis for processor specification, architectural design space exploration, and custom instruction generation.
- Development and design of high-level synthesis tools.
- Development of low-power embedded architectures for digital signal processing applications.
- Compiler development (infrastructure, analysis/optimization passes, backends).
- Development of energy consumption models at the instruction level for embedded processors.
- Design and implementation of embedded systems on FPGA development platforms.

Selection of development projects, prototypes and products

- The **HercuLeS** high-level synthesis environment, commercialized by **Ajax Compilers**. HercuLeS synthesizes software descriptions in either C or a simple n-tuple notation, called NAC (N-Address

Code) to FSMD-style accelerators in portable, vendor-independent, synthesizable VHDL code. HercuLeS is based on the following owned technology:
1) Method of collapsing multiple dependent operations in HDL codes.
2) Method of extracting the control/data flow dependencies in typed assembly language codes.
3) Method of converting static multiple assignment to locally static single assignment code.
4) Graph-based intermediate format for use in software and hardware compilers.
5) System and method for the translation of a textual intermediate representation into hardware description.
Website: http://www.nkavvadias.com/hercules/

- The **YARDstick** custom instruction generator for ASIPs. Performs the automated generation and selection of multiple-input/multiple-output (MIMO) custom instructions for inclusion in ASIP processor models, through analysis and performance estimation of the targeted embedded applications. YARDstick can be retargeted to different architectures and can be used with the gcc compiler and the ArchC simulation infrastructure. It is written in C, C++ and Tcl/Tk (GUI).
  Website: http://www.nkavvadias.com/yardstick/
- The **ByoRISC** customizable and extensible soft core processor family supporting zero-overhead cycle execution of MIMO instructions using a multi-port register file, scalable data forwarding and multiple load/store operations from/to the data memory:
  http://www.nkavvadias.com/misc/byorisc-demo-0.0.1.zip
- **loopgen:** VHDL IP cores for implementing nested loop structures:
  http://nkavvadias.com/eshop/index.php?id_product=10&controller=product
- **xmodz:** Fast hardware implementations of integer modulo:
  http://nkavvadias.com/eshop/index.php?id_product=9&controller=product
- **kdiv** and **kmul:** C/assembly code generators for integer division and multiplication by constant:
  http://github.com/nkkav/kdiv/ and http://github.com/nkkav/kmul/
- **llvmparse:** Portable, standalone, parsers for the textual LLVM IR:
  http://nkavvadias.com/eshop/index.php?id_product=8&controller=product
- **kvcordic:** Universal multi-mode CORDIC computer: http://www.opencores.org/project,kvcordic
- **aprof:** IR profiler tool. http://www.nkavvadias.com/doc/aprof/aprof-README.html
- **hlo:** C-to-C source code optimizer. http://www.nkavvadias.com/doc/hlo/hlo-README.html
- **elemapprox**: Approximating and plotting elementary functions as ASCII or bitmap files for ANSI C, Verilog HDL and VHDL. http://github.com/nkkav/elemapprox/
- The **lcugen** VHDL source code generator for the ZOLC loop control architecture.
- Development of compiler backends (DLX, ByoRISC) for recent GCC versions (3.3.1-3.4.3, 4.0.2, 4.1.0) as well as of newlib and GDB ports.
- Compiler passes and backends for the Machine-SUIF compiler and the SALTO assembly language transformation infrastructure for automatically applying ZOLC optimizations on programmable RISC processors. The **zolcgen** and **tcfggen** passes are available from here:
  http://www.nkavvadias.com/downloads.html.
- Auxiliary SUIF/Machine-SUIF compiler passes for analysis and/or optimization (**bbpart**, **xopreplace**, **bbcount**, **liveanalysis**, **loopstr**, **instrmix**).
- FPGA designs for teaching or demonstration including: line/circle drawing IPs, LCD messaging machine with Picoblaze, two-player game with LED display and UART I/O interface, 2D cellular automata evolution, generic image/video synthesis engine, image viewer, imaging processor.
  For a detailed account of the 2D cellular automata demo shown at a Panhellenic science fair, visit this link: http://nkavvadias.com/blog/2014/05/16/twodimca-fpga/
- ASIC/FPGA designs for customers including radio clock receiver (MSF60/DCF77), biomedical ECG signal processor, FFT IP, parametric signed multiplier (ASIC).

Complete list of publications

A. Journal publications

1. **N. Kavvadias**, P. Neofotistos, S. Nikolaidis, K. Kosmatopoulos and T. Laopoulos, "Measurements Analysis of the Software-Related Power Consumption in Microprocessors," IEEE Transactions on Instrumentation and Measurement, Vol. 53, No. 4, pp. 1106-1112, Aug. 2004.
2. S. Nikolaidis, **N. Kavvadias**, T. Laopoulos, L. Bisdounis, and S. Blionas, "Instruction Level Energy Modeling for Pipelined Processors," Journal of Embedded Computing, Vol. 1, No. 3, pp. 317-324, 2005.
3. **N. Kavvadias** and S. Nikolaidis, "Zero-overhead loop controller for implementing multimedia algorithms," IEE Proceedings – Computers & Digital Techniques, Vol. 152, No. 4, pp. 517-526, Jul. 2005.
4. N. Vassiliadis, A. Chormoviti, **N. Kavvadias** and S. Nikolaidis, "The effect of data-reuse transformations on multimedia applications for application specific processors," International Scientific Journal of Computing, Vol. 4, No. 3, pp. 102-109, 2005.
5. N.D. Vassiliadis, **N. Kavvadias**, G. Theodoridis, and S. Nikolaidis, "A RISC architecture extended by an efficient tightly coupled reconfigurable unit," International Journal of Electronics, Vol. 93, No. 6, pp. 421-438, June 2006.
6. **N. Kavvadias**, V. Giannakopoulou, and S. Nikolaidis, "Development of a customized processor architecture for accelerating genetic algorithms," Microprocessors and Microsystems, Volume 31, Issue 5, pp. 347-359, 1 August 2007. Available online: 12 January 2007.
7. **N. Kavvadias** and S. Nikolaidis, "Elimination of overhead operations in complex loop structures for embedded microprocessors," IEEE Transactions on Computers, Vol. 57, No. 2, pp. 200-214, February 2008.
8. **N. Kavvadias** and S. Nikolaidis, "Scalable register bypassing for FPGA-based processors," Microprocessors and Microsystems, Volume 33, Issues 7-8, pp. 441-452, October-November 2009. Available online: 29 July 2009.
9. T. Stripf, O. Oey, T. Bruckschloegl, J. Becker, G. Rauwerda, K. Sunesen, G. Goulas, P. Alefragis, N.S. Voros, S. Derrien, O. Sentieys, **N. Kavvadias**, G. Dimitroulakos, K. Masselos, D. Kritharidis, N. Mitas, Th. Perschke, "Compiling Scilab To High Performance Embedded Multicore Systems," Microprocessors and Microsystems: Embedded Hardware Design (MICPRO), Volume 37, Issue 8, pp. 1033-1049, November 2013. Available online: 26 July 2013.
10. **N. Kavvadias** and K. Masselos, "Source and IR-level optimizations in the HercuLeS high-level synthesis tool," accepted for publication, International Journal of Innovation and Regional Development, Special Issue on: "Information and Communication Technologies Research and Applications in South East Europe."

B. Publications in conference proceedings

1. **N. Kavvadias**, A. Zanikopoulos, Ch. Voliotidis, S. Kougia, A. Chatzigeorgiou, N. Zervas, S. Nikolaidis, "Power exploration of parallel embedded architectures implementing data-reuse transformations," in Proceedings of the 8th IEEE International Conference on Electronics, Circuits and Systems (ICECS'01), Vol. I, pp. 781-784, Msida, Malta, September 2001.
2. **N. Kavvadias**, A. Chatzigeorgiou, N. Zervas, S. Nikolaidis, "Memory hierarchy exploration for low power architectures in embedded multimedia applications," in Proceedings of IEEE 2001 International Conference on Image Processing (ICIP'01), Vol. 3, pp. 326-329, Thessaloniki, Greece, October 2001.
3. **N. Kavvadias** and S. Nikolaidis, "Parametric Architecture for Implementing Multimedia Algorithms," in Proceedings of the 9th International Conference on Digital Signal Processing (DSP2002), Vol. 2, pp. 1261-1264, Santorini, Greece, July 2002.
4. S. Nikolaidis, **N. Kavvadias**, P. Neofotistos, K. Kosmatopoulos, T. Laopoulos, L. Bisdounis, "Instrumentation set-up for Instruction level power modeling," in Proceedings of 12th

International Workshop on Power Analysis and Timing Modeling, Optimization and Simulation (PATMOS 2002), pp. 71-80, Seville, Spain, September 2002.

5. **N. Kavvadias**, P. Neofotistos, S. Nikolaidis, K. Kosmatopoulos and Th. Laopoulos, "Measurements Analysis of the Software-Related Power Consumption in Microprocessors," in Proceedings of the IEEE Instrumentation and Measurement Technology Conference, Vol. 2, pp. 981-986, Vail, CO, USA, May 2003.
6. S. Nikolaidis, **N. Kavvadias**, T. Laopoulos, L. Bisdounis, S. Blionas, "Instruction Level Energy Modeling for Pipelined Processors," in Proceedings of the 13th International Workshop on Power Analysis and Timing Modeling, Optimization and Simulation (PATMOS 2003), pp. 279-288, Torino, Italy, September 2003.
7. **N. Kavvadias** and S. Nikolaidis, "Tradeoffs in the Design Space Exploration of Application-Specific Processors," in Proceedings of the IFIP WG 10.5 Conference on Very Large Integration of System-on-Chip (VLSI-SoC 2003), pp. 233-238, Darmstadt, Germany, December 1-3, 2003.
8. N. Vassiliadis, A. Chormoviti, **N. Kavvadias**, and S. Nikolaidis, "The Effect of Data-Reuse Transformations on Multimedia Applications for Different Processing Platforms," in Proceedings of the 14th Intl. Workshop on Power and Timing Modeling, Optimization and Simulation, pp. 593-602, Santorini, Greece, September 15-17, 2004.
9. **N. Kavvadias** and S. Nikolaidis, "Application Analysis with Integrated Identification of Complex Instructions for Configurable Processors," in Proceedings of the 14th Intl. Workshop on Power and Timing Modeling, Optimization and Simulation, pp. 633-642, Santorini, Greece, September 15-17, 2004.
10. N.D. Vassiliadis, **N. Kavvadias**, G. Theodoridis, and S. Nikolaidis, "A RISC architecture extended by an efficient tightly coupled reconfigurable unit," in Proceedings of the 1st International Workshop on Applied Reconfigurable Computing 2005 (ARC 2005), pp. 41-49, Algarve, Portugal, February 22-23, 2005.
11. **N. Kavvadias** and S. Nikolaidis, "Hardware support for arbitrarily complex loop structures in embedded applications," in Proceedings of the Design, Automation and Test in Europe Conference (DATE'05), pp. 1060-1061, Munich, Germany, March 7-11, 2005.
12. **N. Kavvadias** and S. Nikolaidis, "Automated Instruction-Set Extension of Embedded Processors with Application to MPEG-4 Video Encoding," in Proceedings of the 16th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2005), pp. 140-145, Samos, Greece, July 23-25, 2005.
13. N. Vassiliadis, A. Chormoviti, **N. Kavvadias**, and S. Nikolaidis, "The Effect of Data-Reuse Transformations on Multimedia Applications for Application Specific Processors," in Proceedings of the Third IEEE International Workshop on Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications (IDAACS 2005), pp. 179-182, Sofia, Bulgaria, September 5-7, 2005.
14. **N. Kavvadias** and S. Nikolaidis, "A flexible instruction generation framework for extending embedded processors," in Proceedings of the 13th IEEE Mediterranean Electrotechnical Conference (MELECON 2006), pp. 125-128, Benalmadena (Malaga), Spain, May 16-19, 2006.
15. **N. Kavvadias** and S. Nikolaidis, "A portable specification of zero-overhead looping control hardware applied to embedded processors," in Proceedings of the 2006 IEEE International Symposium on Circuits and Systems, pp. 1599-1602, Kos, Greece, May 21-24, 2006.
16. **N. Kavvadias** and S. Nikolaidis, "YARDstick: Automation tool for custom processor development," presented at the University Booth of the Design, Automation and Test in Europe Conference (DATE'07), pp. 1-2, Nice, France, April 16-20, 2007.
17. **N. Kavvadias** and S. Nikolaidis, "The ByoRISC configurable processor family," Proceedings of the IFIP/IEEE VLSI-SoC 2008 – International Conference on Very Large Scale Integration, pp. 439-444, Rhodes Island, Greece, October 13-15, 2008.
18. **N. Kavvadias** and K. Masselos, "Efficient hardware looping units for FPGAs," in Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2010), pp. 35-40, Lixouri Kefalonia, Greece, July 5-7, 2010.

19. **N. Kavvadias** and K. Masselos, "NAC: A lightweight intermediate representation for ASIP compilers," Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'11), pp. 351-354, Las Vegas, Nevada, USA, July 18-21, 2011.
20. **N. Kavvadias** and K. Masselos, "Automated synthesis of FSMD-based accelerators for hardware compilation," Proceedings of the 2012 IEEE 23rd International Conference on Application-Specific Systems, Architectures and Processors (ASAP), pp. 157-160, Delft, The Netherlands, July 9-11, 2012.
21. T. Stripf, O. Oey, T. Bruckschloegl, R. Koenig, M. Huebner, G. Goulas, P. Alefragis, N.S. Voros, G. Rauwerda, K. Sunesen, S. Derrien, D. Menard, O. Sentieys, **N. Kavvadias**, G. Dimitroulakos, K. Masselos, D. Goehringer, T. Perschke, D. Kritharidis, N. Mitas, and J. Becker, "A Flexible Approach for Compiling Scilab to Reconfigurable Multi-Core Embedded Systems," Proceedings of the 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (invited paper), pp. 1-8, York, UK, July 9-11, 2012.
22. G. Goulas, P. Alefragis, N.S. Voros, C. Valouxis, C. Gogos, **N. Kavvadias**, G. Dimitroulakos, K. Masselos, D. Goehringer, S. Derrien, D. Menard, O. Sentieys, M. Huebner, T. Stripf, O. Oey, J. Becker, G. Rauwerda, K. Sunesen, D. Kritharidis, and N. Mitas, "From Scilab to Multicore Embedded Systems: Algorithms and Methodologies," Proceedings of the SAMOS XII International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (invited paper), pp. 268-275, Samos, Greece, July 16-19, 2012.
23. J. Becker, M. Huebner, T. Stripf, S. Derrien, D. Menard, O. Sentieys, G. Rauwerda, K. Sunesen, **N. Kavvadias**, K. Masselos, G. Goulas, P. Alefragis, N.S. Voros, D. Kritharidis, N. Mitas and D. Goehringer, "From Scilab To High Performance Embedded Multicore Systems-The ALMA Approach," Proceedings of the 15th Euromicro Conference on Digital System Design, pp. 114-121, September 5-8, 2012, Cesme, Izmir, Turkey.
24. **N. Kavvadias** and K. Masselos, "Design of Fixed-point Rounding Operators for the Latest VHDL Standard," Proceedings of the 2012 Conference on Design and Architectures for Signal and Image Processing (DASIP), pp. 1-8, October 23-25, 2012, Karlsruhe, Germany.
25. **N. Kavvadias** and K. Masselos, "The HercuLeS high-level synthesis environment," Presented at the 23rd International Conference on Field Programmable Logic and Applications (FPL 2013), pp. 1-1, September 2-4, 2013, Porto, Portugal.
26. **N. Kavvadias** and K. Masselos, "Hardware design space exploration using HercuLeS HLS," Proceedings of the 17th Panhellenic Conference on Informatics with International Participation (PCI 2013), pp. 195-202, September 19-21, 2013, Thessaloniki (Salonica), Greece.

C. Book chapters

1. **N. Kavvadias**, V. Giannakopoulou and K. Masselos, "FSMD-Based Hardware Accelerators for FPGAs," in Embedded Systems - Theory and Design Methodology, ISBN 978-953-51-0167-3, ed. by Kiyofumi Tanaka, Intech, pp. 143-166, March 2012.

D. Selected Technical Reports and Deliverables

1. S. Nikolaidis, **N. Kavvadias**, Th. Laopoulos, "Instruction-level power management methodology," Deliverable D8, FP5-IST-2000-30093 EASY (Energy-Aware SYstem-on-chip design of the HIPERLAN/2 standard) project, pp. 1-24, Mar. 2002. (http://easy.intranet.gr/public_deliverables.htm)
2. S. Nikolaidis, **N. Kavvadias**, P. Neofotistos, "Instruction level power measurements and analysis," Deliverable D15, FP5-IST-2000-30093 EASY project, pp. 1-44, Sep. 2002.
3. S. Nikolaidis, **N. Kavvadias**, P. Neofotistos, "Instruction-level power models for embedded processors," Deliverable D21, FP5-IST-2000-30093 EASY project, pp. 1-48, Dec. 2002.
4. G. Dimitroulakos, **N. Kavvadias**, and K. Masselos, "Deliverable 2.1: State-of-the-Art Analysis for Embedded Systems Design," FP7-ICT-248821 ENOSYS (intEgrated modelliNg and synthesis tOol

flow for embedded SYStems design) project, pp. 1-96, June 2010. (http://www.enosys-project.eu)

5. G. Dimitroulakos, **N. Kavvadias**, and K. Masselos, "Deliverable 3.1: State-of-the-Art for Embedded Systems modelling and synthesis," FP7-ICT-248821 ENOSYS project, pp. 1-71, September 2010.
6. G. Dimitroulakos, **N. Kavvadias**, and K. Masselos, "Deliverable 2.3: Methodology for source code optimization using transformations," FP7-ICT-248821 ENOSYS project, pp. 1-58, April 2011.
7. C. Lezos, G. Dimitroulakos, **N. Kavvadias**, and K. Masselos, "Deliverable 3.2: Algorithms for intermediate code generation and hardware resources estimation," FP7-ICT-287733 ALMA (Architecture oriented paraLlelization for high performance embedded Multicore systems using scilAb) project, pp. 1-57, August 2012. (http://www.alma-project.eu)
8. **N. Kavvadias**, and K. Masselos, "Deliverable 3.3: Algorithms for intermediate code optimization," FP7-ICT-287733 ALMA (Architecture oriented paraLlelization for high performance embedded Multicore systems using scilAb) project, pp. 1-26, December 2012. (http://www.alma-project.eu)

E. Non peer-reviewed publications

1. **N. Kavvadias**, "Generating and evaluating application-specific hardware extensions," http://arxiv.org/abs/1403.7380, submitted on 28 Mar. 2014.
2. **N. Kavvadias** and S. Nikolaidis, "Design space exploration tools for the ByoRISC configurable processor family," http://arxiv.org/abs/1403.6632, submitted on 26 Mar. 2014.