Nikolaos K. Kavvadias

Independent Consultant – Research Scientist – Ph.D., M.Sc., B.Sc.

Personal information

Date of birth	April 29, 1977
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Current occupation and work experience

01/14-today	Independent consultant (EDA tools, compilers, system/processor IP, ASIC/FPGA).
09/11-12/13	Researcher for FP7-STREP **ALMA.** Developed **aprof**, a performance estimation tool and **hlo**, a high-level optimizer for Scilab and C.
01/10-12/12	Researcher for FP7-IST **ENOSYS**. Developed **txlcopt**, a source-to-source transformation tool for arithmetic and loop optimizations for ANSI C.
09/08-06/12	Adjunct lecturer at the Dept. of Informatics and Telecommunications of the Univ. of Peloponnese. Courses taught: VHDL, Verilog HDL, Digital Circuit Design, Computer Architecture, Compilers. Supervision of students' theses.
01/05-12/07	Successful grant application for the "Development of a methodology for the design of optimal application-specific processors" funded by the Greek Secretariat of R&T.
09/01-02/03	Researcher for: "**EASY**: Energy-Aware System-on-Chip design of the HIPERLAN/2 standard" (IST-2000-30093) funded by the EU. Co-developed an instruction-level energy consumption model for embedded RISC processors.
08/00-07/01	"Memory management methodology for real-time and low-power embedded multimedia systems" funded by the GSRT. Explored low-power bus encoding schemes and data memory organizations for signal processing algorithms.

Studies

03/03-05/08	Ph.D. from the Physics Dept. of the Aristotle University of Thessaloniki (AUTH), Greece, on "Development of an application-specific processor design methodology".
1999-2002	M.Sc. on Electronic Physics from AUTH, Greece. Grade: **9.41**/10
1995-1999	B.Sc. on Physics from AUTH, Greece. Grade: **8.22/**10

Background knowledge

Prog./design languages	C (excellent), C++, Pascal, Tcl/Tk, TXL, HTML, XML, MATLAB, Processing. Verilog HDL (15 years), VHDL (14 years), SystemC, ArchC, assembly (incl. ARM, MIPS)
Tools/OSes	Xilinx ISE/Vivado, Modelsim, Mentor LeonardoSpectrum, Synopsys VCS/DVE, GHDL, Icarus Verilog, GCC, LLVM, lex, yacc, awk, bash, MachSUIF, binutils, newlib, Graphviz, Boost, SALTO, SPICE, MS Office/Visio, LaTeX, Linux, Windows 95/98/ME/XP/7.
Dev. boards	Spartan-3/3E/3AN Starter Kits, Nios-II DK, ARM Evaluator/Integrator, Parallela.

General information

R&D interests	High-level synthesis, ASIPs, low-power embedded processor design, compilers.
Research outcomes	**HercuLeS** HLS environment, Zero-Overhead Loop Controller (**ZOLC**) architecture, the **ByoRISC** ASIP, **YARDstick** custom instruction generator.
Products and prototypes	HercuLeS, multi-port register file generator, code optimizers, hardware IPs (FFT, 2D cellular automata, loop controllers, motion estimators, biomedical signal processor).
Publications	9 journal and 26 conference publications, 1 book chapter. 103 citations to his work.