cdfg2hdl help

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The usage of the *cdfg2hdl* is as follows:

```
cdfg2hdl [options] input.dot
```

where `options` is one or more of the following:

-d Enable debug output (nothing yet).

-sched-<mode> Perform scheduling on predefined acyclic regions. Valid options for <`mode`>: {`sequential`, `asap`, `naive`}.

-mpint Use multiple-precision arithmetic as implemented by the public domain fgmp library.

-streaming Generate code for hardware units with streaming output(s), generating a sequence of values.

-vhd2vl Generate code more friendly to the "vhd2vl" tool.

-use-rising-edge Use calls to rising_edge for clock event detection.

-use-component-pkg Generate a package "use" for system-wide components.

-ghw Generate a GHDL Waveform file (.ghw) after simulation.

-vcd Generate a VCD waveform file (.vcd) after simulation.

-read-through, -read-first Specify the mode for block RAM synchronous reads (default: read-first).

-blockmem Generate embedded block memories via inference.

-synopsys Use the de-facto Synopsys IEEE library in the generated design code (default).

-ieee Use the normative IEEE library in the generated design code.

-hw-phis Generate hardware for direct support of phi statements.

-fxp-trn-wrap Support for fixed-point arithmetic with truncation (quantization mode) and wrapping (overflow mode). This is the default option.

-fxp-trn-sat Support for fixed-point arithmetic with truncation (quantization mode) and saturation (overflow mode).

-fxp-rnd-wrap Support for fixed-point arithmetic with rounding (quantization mode) and wrapping (overflow mode).

-fxp-rnd-sat Support for fixed-point arithmetic with rounding (quantization mode) and saturation (overflow mode).

-ghdl Generate support files for GHDL simulation (default).

-mti Generate support files for Modelsim simulation.

-quick-abort Abort simulation immediately following the first error.