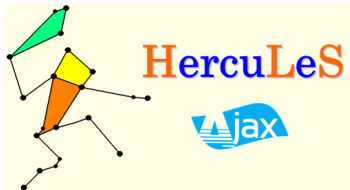


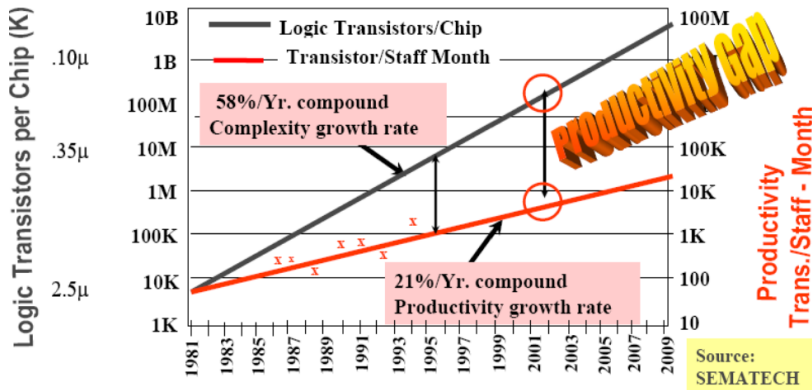
# The HercuLeS HLS environment

Nikolaos Kavvadias  
nkavvadias@ajaxcompilers.com

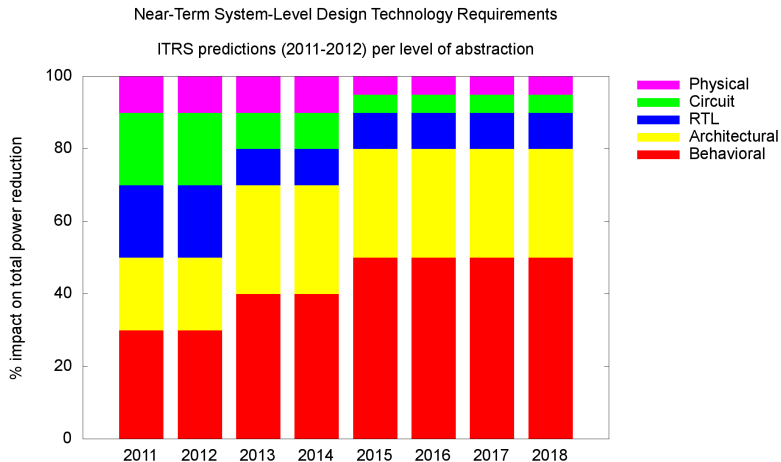
CEO, Ajax Compilers,  
Athens, Greece  
[www.ajaxcompilers.com](http://www.ajaxcompilers.com)



# Technology scales exponentially but humans do not



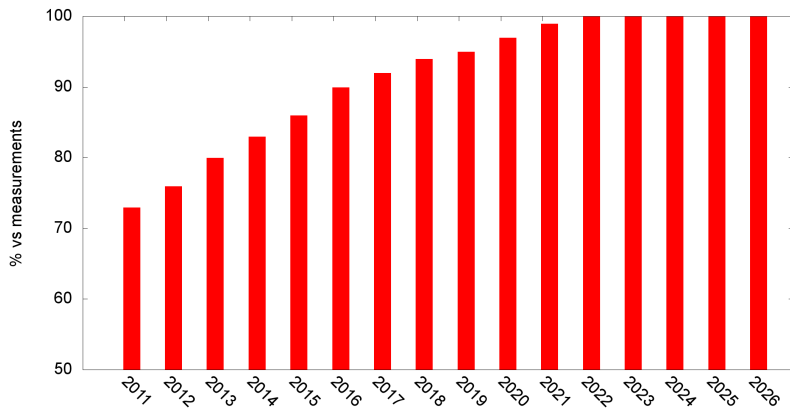
# The 2020 digital system: Reducing power by increasing abstraction



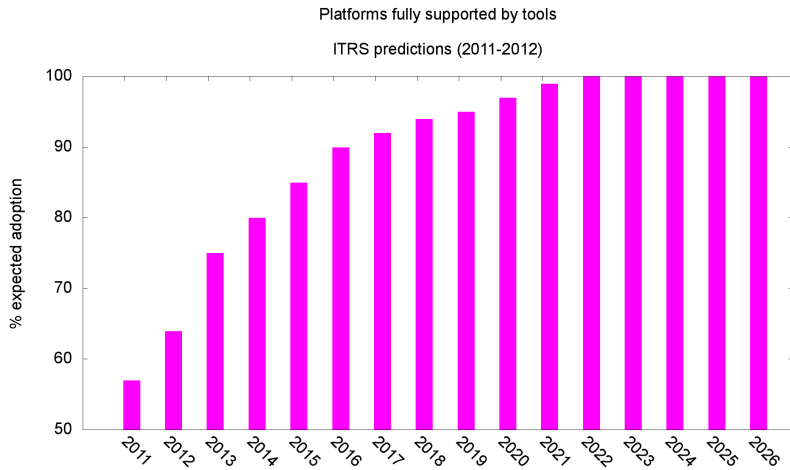
# The 2020 digital system: Highly-accurate estimators are needed

Accuracy of high-level synthesis estimates (performance, area, power, costs)

ITRS predictions (2011-2012)



# The 2020 digital system: Tools for all platforms



# Hardware development is hard (but why?)

**Q** These problems have been solved, right?

**A** No, they have not! They are still open and relevant

## ■ **Technology partner?**

- Your time-to-market margin is shrinking for each new product
- You don't have zillions of employees. Your human resources are limited
- Eventually you will run onto your monetary ceiling
- If you don't act now, you will be overridden by competition which uses novel approaches

## ■ **Investor?**

- EDA (Electronic Design Automation) is a great market
- Steady growth of 10-15% per year
- EDA is core technology in rapidly growing markets such as mobile, medical, space, robotics
- Greece lags far behind; high-tech mid-scale production is strategic

# High-level synthesis (HLS) comes to the rescue

- Adoption of a high-level design and synthesis methodology imposing user entry from a raised level of abstraction
  - 1 Hide low-level, time-consuming, error-prone details
  - 2 Drastically reduce human effort
  - 3 End-to-end automation from concept to production

**HLS** An algorithmic description is automatically synthesized to a customized digital embedded system

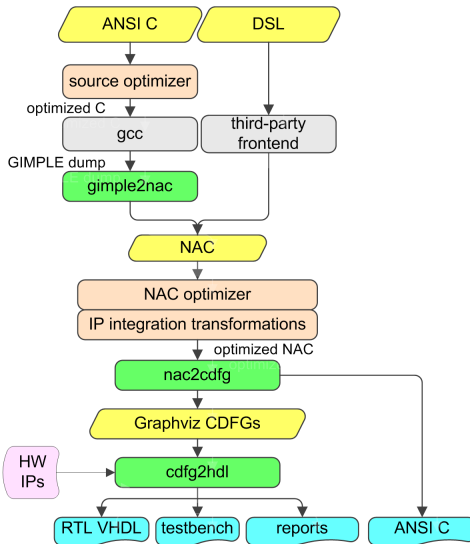
- **HercuLeS**: An easy to use HLS environment
- Targets both hardware and software engineers/developers
  - 1 ASIC/SoC developers, FPGA-based/prototype/reference system engineers
  - 2 Algorithm developers (custom HW algorithm implementations)
  - 3 Application engineers (application acceleration)

# Five things we already do better than competition

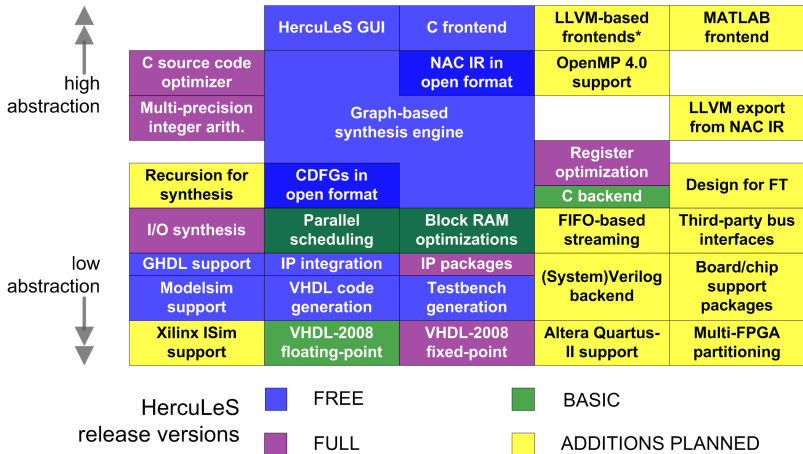
- 1** Competition tools cannot be extended
  - In HercuLeS new frontends (e.g. for domain-specific languages), analyses and optimizations are easy to add
- 2** Insufficient and opaque representations
  - HercuLeS uses open specifications and formats
  - Its intermediate representation is NAC, a universal typed-assembly language
  - Program graphs expressed in the open Graphviz format
- 3** Automatic character I/O, dynamic memory allocation and GMP arithmetic are not supported
  - HercuLeS is the first HLS tool to support these features
- 4** Mandating the use of code templates
  - HercuLeS does not rely on code templates since it uses a graph-based backend
- 5** Succumbing to vendor and technology dependence
  - The generated HDL is human-readable and vendor- and technology-independent; portable across FPGA and ASIC



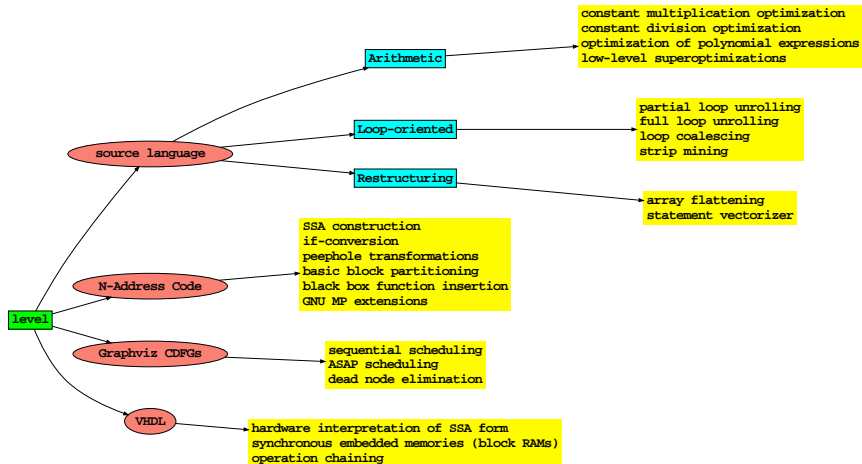
# The HercuLeS flow



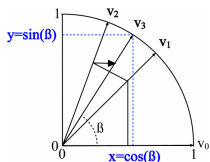
# Features



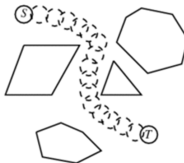
# The optimization space of HercuLeS



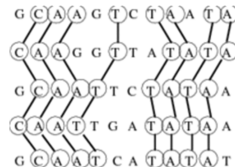
# IPs generated by HercuLeS



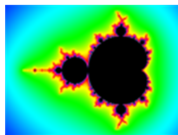
Approximations



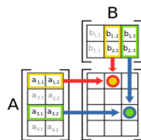
Path planning



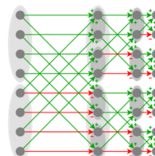
Pattern matching



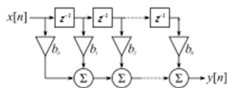
Graphics



Matrix processing



Transforms



Filters

$$X_k = \sum_{n=0}^{N-1} e^{-2\pi i k \cdot (n/N)} x_n$$

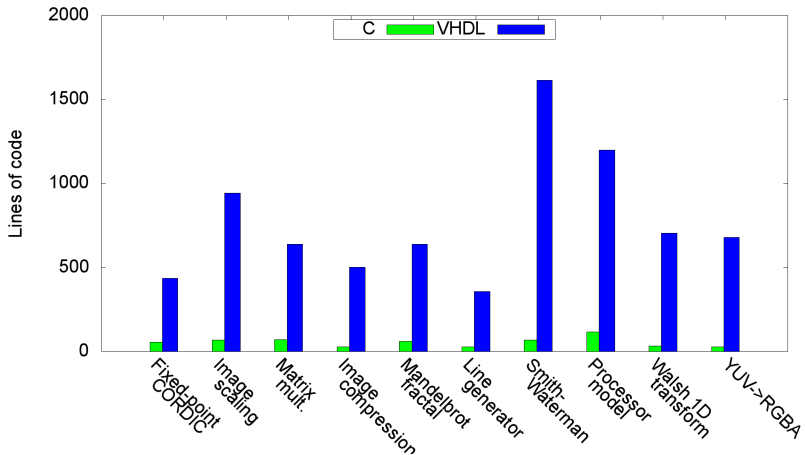
Spectrum analysis

$$x_i^{(k+1)} = \frac{1}{a_{ii}} (b_i - \sum_{j=1, j \neq i}^n a_{ij} x_j^{(k)})$$

Linear systems



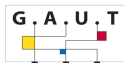
# More than 10x productivity increase!



# The HLS landscape



cādence CyberWorkBench®



LegUp

SYNOPSYS®



Jacquard  
COMPUTING INC



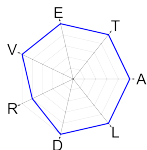
XILINX  
ALL PROGRAMMABLE™

bluespec®

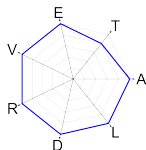


Calypto  
Catapult®

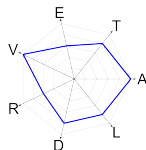
# HLS tools comparison (Abstraction; Types; Explore; Verify; Results; Documentation; Learning)



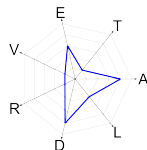
CatapultC



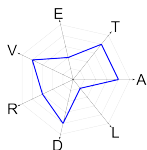
Vivado HLS



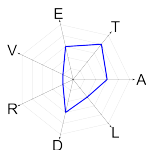
Symphony C



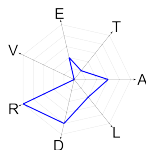
ROCCC



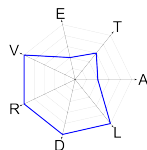
C-to-Silicon



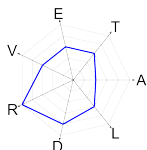
ImpulseC



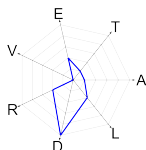
Bluespec



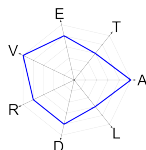
System Generator



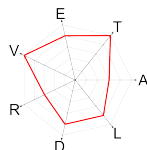
GAUT



SPARK



LegUp



HercuLeS

# Against competition

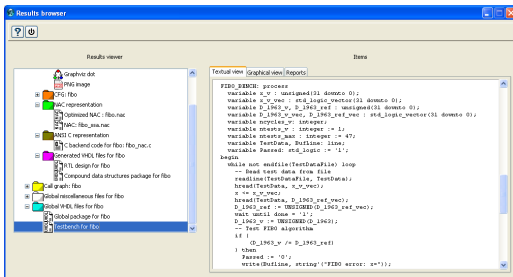
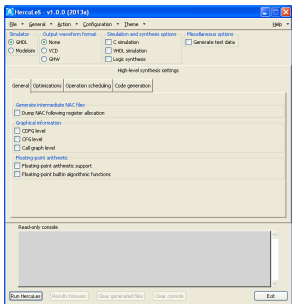
- Preliminary results against Vivado HLS 2013.2 on Virtex-6 and/or Kintex-7 (\* KC705 development board; XC7K70TFBG676-2 FPGA device)

Benchmark	Vivado HLS			HercuLeS		
	LUTs	Regs	Time (ns)	LUTs	Regs	Time (ns)
*Array sum	<b>83</b>	<b>172</b>	<b>60.5</b>	164	205	68.327
Bit reversal	67	<b>39</b>	72.0	<b>42</b>	40	<b>11.6</b>
*Radix-2 division	<b>218</b>	<b>226</b>	63.6	318	332	<b>30.6</b>
Edge detection*	<b>246</b>	<b>130</b>	1636.3	680	361	<b>1606.4</b>
Fibonacci series	138	<b>131</b>	<b>60.2</b>	<b>137</b>	197	102.7
FIR filter	<b>102</b>	<b>52</b>	<b>833.4</b>	217	140	2729.4
*FIR filter	<b>89</b>	<b>114</b>	1027.1	606	540	<b>393.8</b>
Greatest common divisor	210	98	<b>35.2</b>	<b>128</b>	<b>93</b>	75.9
Cubic root approx.	<b>239</b>	207	<b>260.6</b>	365	<b>201</b>	400.5
Population count	<b>45</b>	<b>65</b>	<b>19.4</b>	53	102	26.1
Prime sieve*	525	595	6108.4	<b>565</b>	<b>523</b>	<b>3869.5</b>
*Sierpinski triangle	<b>130</b>	296	<b>10538.2</b>	206	<b>227</b>	22402.9



# The HercuLeS GUI

- Bundled with HercuLeS v1.0.0 (2013a) released on June 30
- Specify code generation, simulation and synthesis options
- Includes embedded results viewer



# Summary

- ☞ HercuLeS is an extensible HLS environment for hardware and software engineers
- Straightforward to use from ANSI C, generic assembly (NAC) or custom DSLs to producing compact VHDL designs with competitive QoR
- Product information
  - HercuLeS GUI for specifying code generation, simulation and synthesis options
  - Commercial distribution: <http://www.ajaxcompilers.com>
  - Technical details: <http://www.nkavvadias.com/hercules/>
  - **FREE** version available:  
<http://www.nkavvadias.com/temp/index.php>
  - **FREE**, **BASIC**, and **FULL** software licensing schemes (2013.a version)

Thank you

for your time and interest!