HercuLeS
Automated synthesis of FSMD-based accelerators for hardware compilation

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What is HercuLeS?
An extensible, high-level synthesis (HLS) environment for whole-program hardware compilation that allows pluggable optimizations and analyses

- Overcomes limitations: (1) nonstandard source languages, (2) insufficient representations, (3) maintenance difficulties, (4) mandating the use of code templates, (5) vendor dependence
  1. Connects to GIMPLE/GCC as a frontend scenario
  2. Uses the succinct NAC intermediate representation
  3. Optimizations added as self-contained external modules
  4. Hardware compilation engine is entirely graph-based
  5. The generated HDL is human-readable and completely vendor- and technology-independent

Automation for FSMD-based accelerators
- The generated accelerators adhere to an extended FSMD model of computation
- This model allows for:
  - Synchronous embedded memory accesses
  - Intermodule communication (hierarchical FSMDs)
  - Hardware-optimizing transformations such as operation chaining
  - Automatic IP integration
- More on optimizations:
  - Optimizations possible at the source, NAC, graph and VHDL level
  - Pluggable loop-oriented transformations, advanced arithmetic optimizations, graph rewriting, VHDL "hacks"

Example: Prime factorization

```c
void pfactor(uint x, uint *outp) {
  uint i=2, nx;
  while (i < x) {
    if ((x/i) == x/i) {
      i = i + 1;
    } else {
      nx = x/i;
      'outp = i;
    }
  }
}
```

Hierarchical FSMDs

Chaining

Against academic tools

Performance of FSMDs

Additional information
HercuLeS is marketed by Ajax Compilers. Unl.
Its inaugural release is expected in Q3, 2012 (IP design services are already provided).

New features include: support for IEEE-754/custom floating-point arithmetic and source-level optimization.

http://www.nkavvadias.com/hercules

http://www.nkavvadias.com/cgi-bin/hec.cgi

http://www.nkavvadias.com/hercules/algorithmic-ips.html